UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/044,974	01/15/2002	Eric C. Fox	5791	2770

7590 03/21/2003

Dorsey & Whitney LLP
Suite 300 South
1001 Pennsylvania Avenue, N.W.
Washington, DC 20004

EXAMINER
TRAN, TAN N

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/044,974	FOX, ERIC C.	
	Examin r	Art Unit	
	TAN N TRAN	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendmend filed on 01/07/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,21 and 22* is/are pending in the application.

4a) Of the above claim(s) *19 and 20* is/are withdrawn from consideration.

5)☒ Claim(s) *14-18,21* is/are allowed.

6)☒ Claim(s) *1-5,7-13,22* is/are rejected.

7)☒ Claim(s) *6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 12,13,22 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification does not disclose the CMOS circuitry process type well is formed to a greater depth than a depth of the first well as recited in claim 12.

The specification does not disclose the CMOS process type well is formed to a greater concentration than the second concentration as recited in claim 13.

The specification does not disclose an epi layer of the first conductivity type in a second concentration, the second concentration being less than the first concentration; a first well of a second conductivity type formed in the epi layer as recited in claim 22. Note lines 5-15, page 9 in the specification of application just prefer to Figs. 1,2,3, but not prefer to fig. 5 of Application's invention.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10-13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 10,12,13, lines 7,8, "the CMOS circuitry includes at least one FET formed in a CMOS process type well of the first conductivity type" is unclear as to whether it is being referred to the CMOS circuitry includes at least one FET formed in a first well 74 as drawing 3 of applicant's invention.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the CMOS circuitry process type well is formed to a greater depth than a depth of the first well as recited in claim 12, the CMOS process type well is formed to a greater concentration than the second concentration as recited in claim 13, an epi layer of the first conductivity type in a second concentration formed on the substrate, the second concentration being less than the first concentration; a first well of the first conductivity type in a third concentration as recited in claim 21, and an epi layer of the first conductivity type in a second concentration, the second concentration being less than the first concentration; a first well of a second conductivity type formed in the epi layer as recited in claim 22 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1,7-11 rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe (6,448,104) (of record).

With regard to claims 1,10, Watanabe discloses a sensor formed in a substrate 100 of a first conductivity type in a first concentration p- comprising: CMOS circuitry 3 to control the sensor; a first well 110 of the p^- type in a second concentration formed in the substrate 100, the second concentration being greater than the first concentration; and a photodiode region 130 of a n+ type formed completely within the first well 110; (Note figs. 10B,10C of Watanabe). It is inherent that the CMOS circuitry includes at least one FET formed in a CMOS process type well

of the p- type because the conventional CMOS circuitry normally comprising the n-channel FET and p-channel FET.

With regard to claim 7, it is inherent that a gate electrode insulatively spaced over the first well 110 and disposed to control a transfer of charge between the photodiode region 130 and predetermined region 131 of the second conductivity type because the gate electrode controls the charges that move from the source region to the drain region. Note figs. 10A-10C of Watanabe.

With regard to claim 8, Watanabe discloses the predetermined region 131 of the second conductivity type is formed in the first well 110. Note fig. 10C of Watanabe.

With regard to claim 9, since Watanabe discloses the substrate 100 having a first concentration and having first intrinsic potential and the well 110 having second concentration that is greater than the first concentration and a second intrinsic potential. It is inherent that the first and second intrinsic potentials induce a field between the substrate 100 and the first well 110 that repels photo generated charge from drifting from the substrate 100 into the first well because such structure of Watanabe is formed the same that of applicant, so the structure of Watanabe has the same functions as structure of applicant.

Applicant's claim 11 does not distinguish over Watanabe references regardless of the process used to form the CMOS process type well and the first well because only the final product is relevant, not the process of making such as "single processing step, the single processing step including one of ion implantation and dopant diffusion".

Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal

with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases, as the above case law makes clear.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe (6,448,104) (of record) in view of Lee et al. (6,297,070).

With regard to claim 2, Watanabe discloses a sensor formed in a substrate 100 of a first conductivity type in a first concentration (p^-) comprising: CMOS circuitry 3 to control the sensor; a first well 110 of the p^- type in a second concentration formed in the substrate 100, the second concentration being greater than the first concentration; and a photodiode region 130 of a n+ type formed completely within the first well 110. (Note figs. 10B, 10C of Watanabe).

Watanabe does not disclose a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate.

However, Lee et al. discloses a pinning layer 22 of the first conductivity type formed to a shallow depth in the photodiode region 32 and electrically coupled to the substrate 2.

Therefore, it would have been obvious to one of ordinary skill in the art to form the Watanabe's device having a pinning layer of the first conductivity type formed to a shallow depth in the photodiode region and electrically coupled to the substrate such as taught by Lee et al. in order to improve the blue response, reduce lag and minimize the dark current characteristics of the active pixel sensor.

With regard to claims 3,5, Watanabe discloses gate electrode insulatively spaced over the first well 110 and substrate 100, and disposed to control a transfer of charge between the photodiode region 130 and a predetermined region 131 of the second conductivity type. (Note fig. 12C of Watanabe).

With regard to claim 4, Watanabe discloses the predetermined region 131 of the second conductivity type is formed in the first well 110. (Note fig. 12C of Watanabe).

Allowable Subject Matter

6. Claim 6 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 6 is allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as a second well of the first conductivity type in the second concentration, wherein the predetermined region of the second conductivity type is formed in the second well as recited in claim 6.

7. Claims 14-18,21, are allowable over the prior art of record, because none of these references disclose or can be combined to yield the claimed invention such as a photodiode region of the second conductivity type formed in the second well as recited in claim 14, an epi layer of the first conductivity type in a second concentration formed on the substrate, the second concentration being less than the first concentration; a first well of the first conductivity type in a third concentration as recited in claim 21.

Conclusion

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Tan Tran whose telephone number is (703) 305-3362. The examiner can normally be reached on M-F 8:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the

organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for after final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TT

Mar 2003

Minh Loan Tran
Primary Examiner